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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application Number	10/720,672
Filing Date	November 25, 2003
First Named Inventor	NOVAKOVSKY, Alexander
Group Art Unit	~~2183~~ 2825
Examiner Name	~~Not yet known~~ TUYEN TO
Attorney Docket Number	P-5667-US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (where appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
TT	A	Jolly, Simon; Parashkevov, Atanas; McDougall, Tim: "Automated Equivalence Checking of Switch Level Circuits", pgs. 299-304; DAC 2002, June 10-14, 2002, New Orleans, Louisiana, USA.	☐
TT	B	Kuehlmann, A.; Srinivasan, A.: "Verity - a formal verification program for custom CMOS circuits": IBM Journal of Research & Development, Jan-Mar 95, Vol. 39, Issue 1 of 2, p. 149, 17p., 3 charts, 9 diagrams	☐
TT	C	Fischer et al. "Abstraction of Schematic to High Level HDL. Design", Technology, Intel Israel (74) Ltd. ICCAD 1990, pp. 90-96	☐
TT	D	Kam et al., "Comparing Layouts with HDL Models: A Formal Verification Technique", IEEE, 1992, pp. 588-591	☐
TT	E	Kam et al., "State Machine Abstraction from Circuit Layouts using BDD's: Application in Verifications and Synthesis", IEEE, 1992, pp. 92-97	☐
TT	F	Lester et al.: LIP6/ASIM Laboratory, University Pierre et Marie Curie-Paris: "Yagle, a second generation functional abstractor for CMOS VLSI Circuits", 1998, pp. 265-268	☐
TT	G	Bryant :"Boolean analysis of MOS circuits ", IEEE Transaction on computer-aided design, Vol. CAD-6, No. 4 July, 1987, pp. 634-649	☐
TT	H	Bryant, "Extraction of gate level models from transistor circuits by four valued symbolic analysis", IEEE, 1991, pp. 350-353	
			☐

Examiner Signature	Tuyen To	Date Considered	10/20/2005

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